

Capturing the Edge AI market

Electronic devices, and the chips in them, are getting smaller and smaller in size every year, while being expected to do more and more at the same time. Nanoveu (ASX:NVU) recently acquired a semiconductor company with Intellectual Property (IP) that enables a very novel approach to bringing Artificial Intelligence (AI) to devices at the Edge of the Internet, such as cameras, mobile phones, robots etc.

EMASS is a significant opportunity

Nanoveu acquired Singapore-based EMASS, a fabless semiconductor company, that has developed an AI-focussed System-on-a-Chip (SoC) with 20x the power efficiency of competing products. Once fully developed, EMASS' technology will reside in SoC's that can be installed in Edge devices where they perform very specific AI inference tasks in a way that is extremely energy efficient.

This extreme processing efficiency opens up countless global industries and device markets where EMASS could make a big difference, including in autonomous vehicles, wearables, robotics and medical devices. These markets combined total well in excess of US\$100bn in value and are growing fast.

Semiconductor-focused management team

Following the acquisition of EMASS, that saw founder Dr. Mohamed Sabry Aly transition to Nanoveu, the company has also recently retained semiconductor industry veteran Mark Goranson to head up the new semiconductor division. With extensive stints at leading, global semiconductor companies, including Intel and ON Semiconductor, we believe Mr. Goranson brings a wealth of experience in semiconductor manufacturing and commercialisation, which may expedite EMASS' time-to-market with initial products.

Recent M&A deals imply substantial share price upside

On 10 February 2025, Dutch semiconductor incumbent NXP Semiconductors acquired Silicon Valley-based Edge AI chip developer Kinara for US\$307m (A\$482m). This deal followed a number of other acquisitions and listings of Edge AI chip companies with valuations ranging from US\$80m to more than US\$500m. In our view, EMASS has better performance metrics than Kinara's Edge AI solution, which provides an indication of Nanoveu's future value. While it's too early to incorporate these recent M&A valuations into our Nanoveu valuation just yet, we do see a clear M&A scenario for EMASS once the IP is close to being commercialised. For now, we value Nanoveu at A\$0.17 per share, based on the average of its ASX-listed semiconductor peer group (see page 16). Please see page 17 for the key share price catalysts and page 18 for the key risks.

Share Price: A\$0.042

ASX:NVU

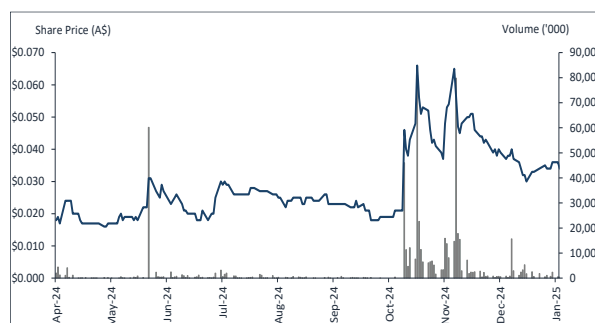
Sector: Technology

27 February 2024

Market cap. (A\$ m)	31.2
# shares outstanding (m)	742.4
# shares fully diluted (m)	1,146.7
Market cap ful. dil. (A\$ m)	48.2
Free float	100%
52-week high/low (A\$)	0.081/0.016
Avg. 12M daily volume ('000)	3,171
Website	https://nanoveu.com

Source: Company, Pitt Street Research

Share price (A\$) and avg. daily volume (k, r.h.s.)



Source: Refinitiv Eikon, Pitt Street Research

Valuation metrics	
Valuation (A\$ per share)	A\$0.17

Source: Pitt Street Research

Disclosure: Pitt Street Research directors own shares in Nanoveu.

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The Nanoveu Investment Case

1. **Nanoveu's recently acquired EMASS technology offers enormous potential.** It will enable devices using the technology to perform complex computations without relying on cloud processing. EMASS' chip has 13 million AI parameters and is capable of 30 Giga-Operations per second, or 10 trillion AI operations per second per watt.
2. **EMASS will consequently ensure faster and smoother actions** and user experiences in environments of all powers and bandwidths. It has 20x energy efficiency compared to competitors, with <2 milliwatts power consumption.
3. **EMASS' chip compares very well to competing products** due to the ultra-low-power operation that can reduce energy consumption in devices, the tiny silicon footprint of the chipset, which lowers manufacturing costs and its carbon footprint. And, by processing AI tasks on device, it reduces reliance on power-hungry data centres and network bandwidth, improving security and reducing latency.
4. **The market potential is very high** with most forecasters predicting an Edge AI market size of at least US\$100bn by 2030. Some even predict a market of more than US\$200bn in size by 2030.
5. **EMASS' product pipeline is very promising.** With an extensive innovation pipeline, the company has positioned itself as a frontrunner in the development of next-generation SoC technologies for Edge AI applications.
6. **Nanoveu's Management team.** NVU's management team offers a wealth of experience in listed companies generally, in technology companies as well as in academic research that has conceived innovations that have been brought to market. The EMASS acquisition will see its CEO Professor Mohamad Sabry Aly, a Stanford-trained engineer whose pioneering research has driven advancements in SoC design. Nanoveu recently appointed Mark Goranson as CEO of Semiconductor Operations. Mr. Goranson has an extensive track record in semiconductor manufacturing and commercialisation, including stints at Intel, ON Semiconductor and Freescale Semiconductor.
7. **Nanoveu's legacy business, EyeFly3D and Nanoshield, present lucrative opportunities too.** We think investors may be disregarding the potential of Nanoveu's existing business as the perception post-Covid was that sales would stagnate or slow. But Nanoshield is now targeted towards solar panels and submerged surfaces. With potential commercial deals on the horizon, the legacy business should be able to fund itself and potentially EMASS as well going forward. See Appendix I.
8. **We believe Nanoveu is seriously undervalued.** Even though EMASS' technology is at a relatively early stage, we believe it is undervalued compared to its ASX semiconductor peers as well as international peers in the Edge AI space, such as Kinara that was recently acquired for ~A\$500m while also being at an early stage of development. We believe Nanoveu should be valued at A\$0.17 per share in the medium term, with further upside as the technology gets commercialised (see page 16).
9. **The main share price catalysts for Nanoveu's share price** will be announcements around the further development and commercialisation of EMASS' technology, such as tape-outs of new iterations of the chip, sampling by prospects, collaborations with prospects and industry players, license agreements etc.

EMASS delivers Artificial Intelligence at the Edge

Nanoveu was established in 2012 and licensed Intellectual Property (IP) that enabled it to create EyeFly3D in 2013. The company listed on the ASX in November 2018 and developed Nanoshield across the 2020s starting during the pandemic.

The company announced the acquisition of Singapore-based EMASS in October 2024, which will be the primary focus of this report. EMASS is developing an ultra-low power semiconductor System-on-a-Chip (SoC) for Edge AI (Artificial Intelligence) applications.

We will also address EyeFly3D later in this report because the company will be carrying on this business alongside EMASS.

EMASS gives Nanoveu exposure to high-growth AI markets

In acquiring EMASS, Nanoveu has given itself exposure to the quickly growing Artificial Intelligence market.

In acquiring EMASS, Nanoveu has taken itself to the next level, offering it exposure to a quickly growing Artificial Intelligence (AI) market. As AI becomes more and more entrenched in life, so will 'Edge' solutions that make AI at the Edge possible, such as wearables and smart home systems.

Nanoveu was able to retain EMASS' founder Dr. Mohamed Sabry Aly in the acquisition. Going forward, Dr. Aly will be driving EMASS' Research & Development efforts.

Once fully developed, EMASS' technology will be offered directly to manufacturers of Edge devices, including wearables, fitness trackers, drones and advanced IoT devices.

EMASS in a nutshell

EMASS is a fabless semiconductor design company, specialising in ultra-low power SoC solutions for Artificial Intelligence 'at the Edge'.

EMASS is a fabless semiconductor design company that was founded in 2020 by Prof. Dr. Mohamed Sabry Aly, at Nanyang Technological University in Singapore. Dr. Aly completed postdoctoral work at Stanford, where his research contributed to a transformative US\$75m DARPA project. EMASS was incubated at Nanyang to design and develop high-performance, ultra-low power semiconductor System-on-a-Chip (SoC) solutions.

EMASS' technology entails ultra-low power SoC solutions for AI 'at the Edge'. These are semiconductors (chips) that enable processing of data to be done at close proximity to data-generating sensors rather than in centralised data centers.

EMASS' current suite of IP includes five core technologies in SoC's, covering algorithmic transformation, hardware support, system architecture and AI-specific hardware accelerators. These SoC's are 20x more energy efficient compared to competitor chips and can handle 13 million AI parameters and process them at 30 Giga Operations per second (GOPS). It does this at less than 2 milliwatts of power consumption.

EMASS' SoC's are based on the Reduced Instruction Set Computing (RISC-V) architecture, known for its simplicity, extensibility and low power consumption.

Before we jump deeper into the potential of EMASS' technology, let's have a quick look at how and where this technology can be deployed, i.e. SoC's in Edge devices.

Several key benefits compared to competing products.



Edge computing has many advantages compared to Cloud computing.

Edge computing is different from cloud computing in several ways

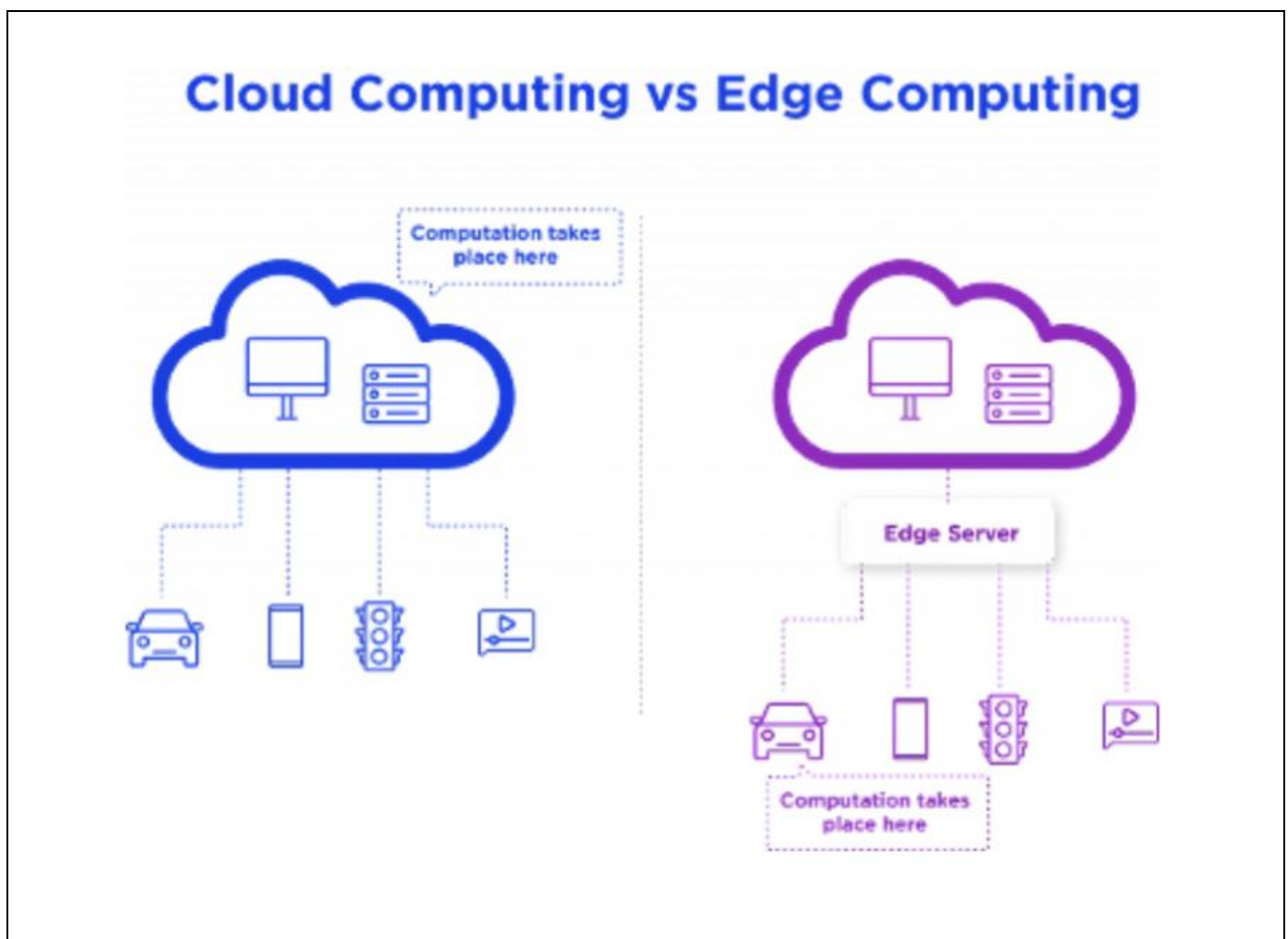
Edge computing is so-called because of where the data that is generated is being processed – on the device or sensor that also generated the data to begin with. The term ‘Edge’ refers to the edge of the Internet where many billions of connected devices reside.

Edge computing enables faster data processing (on the actual Edge device) and ensures better data sovereignty by avoiding the need for data to travel between servers and other connected devices to get processed.

By contrast, Cloud computing is done in ‘The Cloud’, using data centres with global servers. These typically tend to be far removed from the device connected to the Internet and are dependent on Internet connections to operate (Figure 1). Compared to Edge computing, Cloud computing is typically slower, uses much more bandwidth and more power while being less secure.

However, Cloud computing enables substantially larger amounts of data to be processed in the same timeframe.

Figure 1: Cloud vs Edge Computing



Source: Nanoveu



An SoC is a highly integrated semiconductor that consolidates all essential components of a computer in a single chip.

EMASS' SoC enables complex, computationally intensive tasks to be done and done 'at the edge'.

EMASS' SoC have demonstrated many benefits compared to their peers, including higher performance and energy efficiency.

SoC's are miniaturised computer systems with a specific task

A System-on-a-Chip is a highly integrated semiconductor that consolidates all essential components of a computer (such as a CPU, GPU, memory, network communication and input/output controls) in a single chip. This integration allows devices to perform complex tasks, such as AI acceleration, data processing, 3D graphic rendering and wireless communication in a much smaller, more power-efficient chip.

The SoC was first developed in the early 1970s and was first used in a liquid crystal display (LCD). Today's SoC's are commonly used in portable devices, like smartphones, wearables, medical and IoT devices, where space is limited and efficient use of power is critical due to battery-size restrictions.

SoC's have many use cases because they can perform multiple complex tasks while consuming minimal energy. This makes SoC's ideal for devices that need to process data quickly with low power consumption.

The demand for more efficient SoC's is rapidly expanding as technologies like AI, 5G, 3D rendering and VR (Virtual Reality) demand more and more processing power from increasingly smaller Edge devices.

EMASS' technology resides in SoC's that are installed in Edge devices where they perform very specific AI-focussed computing tasks.

Ultra-low power Artificial Intelligence at the Edge

EMASS' SoCs enable complex, computationally intensive tasks to be done and done 'at the edge', which reduces the need to send large amounts of data to the cloud for processing, saving bandwidth and ensuring smoother and more efficient processing, especially in low-power and low-bandwidth requirements.

EMASS' SoC has the potential to bring advanced AI capabilities to applications where power supply and computational power is typically low and allows devices to perform complex tasks by consuming very little power on battery-operated or energy-sensitive applications.

The benefits of EMASS are plentiful

Compared to industry peers, EMASS SoCs have demonstrated:

- **High computational efficiency** (30 Giga Operations per second or 30 billion operations/second). The next best competitor runs at 6.4 GOPs. This translates to over 10 trillion AI operations per second per watt, compared to the current <2 trillion operations per second for the same product category,
- **Superior Power Efficiency:** EMASS' chip operates at an average of 0.1mW (Milliwatt) with a maximum power usage of 10mW, making it the most power-efficient SoC on the market and suitable for next-generation portable devices (such as wearables and IoT devices) where battery life and low power consumption are critical,
- **High memory capacity** with 4 Megabytes of memory on board on a chip with <10mm² footprint,
- **Supporting up to 13 million simultaneous AI parameters,**



- **Integrated software optimisation:** RISC-V open-source architecture allows full customisation of the chip design to match end-user requirements, and
- **High energy efficiency given their design.**

We also note that EMASS' SoCs are environmentally friendly due to the ultra-low-power operation that can reduce energy consumption in devices as well as the tiny silicon footprint of the chipset, which lowers manufacturing costs and carbon impact. Additionally, EMASS' solution reduces reliance on power-hungry data centres and network bandwidth, improving security and reducing latency.



EMASS does Edge AI differently: A look under the hood

As we will discuss in this chapter, EMASS' chip centers around 4 key attributes:

- smart chip design,
- clever use of new Non-Volatile Memory (NVM) technology,
- enhanced memory compression techniques, and
- highly efficient processing workflow.

Chip design is dictated by Edge AI requirements

Given that EMASS' technology caters to Edge devices that need AI capabilities, there are two principles that dictate the chip design:

- Firstly, you don't want to waste energy by having to transmit data back and forth to the Cloud for processing. Instead, you want to process the data close to where it is generated, i.e. on the Edge device itself.
- Secondly, Edge devices are generally much smaller than centralised devices, so the chip real estate (form factor) is much smaller. This means the chip design will have to be much smaller, including the batteries and other chip components, such as the memory modules, processors etc.

Because of these restrictions, EMASS has designed its chip in a very specific way:

1. Only do the computations that really matter.
2. The application is extremely compressed to limit the use of memory capacity and processing power. We will elaborate on this later on.
3. All components that are not needed to perform the specific task at that specific time are turned off to save energy.

For instance, when the chip is capturing data, you don't need the AI accelerator running. And when data capture is complete, you don't want the I/O (input/output) peripherals to be active, so they are turned off, but you activate the AI functionality.

Through this delicate switching between functionalities, also known as power gating, any unnecessary consumption of energy, no matter how small, can be eliminated.

In order to do this, you need the right technology, the right chip architecture and the right software to manage this workflow, which is what EMASS has brought together in its chip.

Commercial price point further determines the chip architecture

The architecture and design of the chip is not just determined by the intended use and the available chip real estate, it is also determined by the price point that EMASS is targeting for its chip.

The price of the chip when it becomes commercially available needs to be relatively low in order to maximise the uptake by customers. EMASS is targeting an Average Selling Price (ASP) of US\$7-10, i.e. the price it will charge OEMs and other off takers. This means EMASS can't use the most advanced technology, because that would result in a price point in excess of US\$50. So, the company aims to manufacture its chips at the 22nm technology node or other cost-effective (at scale) nodes.

Edge AI principles dictate the chip design.

Power gating helps limit energy consumption.

Targeting a wholesale price point of US\$7-10 per chip.



The use of new types of NVM has many benefits.

The fact that the chip will not be manufactured using so-called leading edge technology, i.e. below 7nm, implies two things:

1. At the 22nm technology node, any innovation has to come from the design itself as performance improvements can't come from scaling down to small resolutions, which would give speed and power consumption benefits.
2. Secondly, EMASS will need to use new types of Non Volatile Memory (NVM), such as MRAM (Magnetoresistive Random Access Memory) or ReRAM (Resistive RAM) at 22nm (or a more advanced by depreciated technology node). NVM doesn't lose its stored data if the power is turned off. These new types of NVM have much higher reads speeds than the current industry workhorse NVM, Flash memory, i.e. 20-30 nanoseconds for MRAM versus several microseconds for Flash memory, which is a massive difference.

MRAM and ReRAM at 22nm are also much denser than SRAM that doesn't scale down cost-effectively below 40nm. As a consequence, memory capacity can be much higher with these new NVM's for the same amount of chip surface used. EMASS will still need a little bit of volatile Static RAM (SRAM) as working memory given that NVM has much lower endurance than volatile memory. But it will need much less SRAM per chip compared to a situation where no MRAM or ReRAM is available.

Another benefit of using MRAM or ReRAM is that the wake-up time for these new types of NVM is much faster than for Flash memory, i.e. 1 or 2 microseconds versus 10s or 100s of milliseconds, which is at least 10,000x faster. This much faster wake-up time further contributes to the chip's speed.

In the current iteration of EMASS' chip there is 16Mbit of MRAM and just 1 Mbit of SRAM incorporated. However, EMASS is replacing MRAM with ReRAM.

ReRAM will make EMASS' chips more durable

EMASS has used MRAM in its chip design, which is a newly evolved type of NVM that stores data through magnetic states instead of electrical charges.

MRAM is, theoretically, renowned for high endurance, but has several major drawbacks, such as high sensitivity to magnetic fields. Companies that previously manufactured MRAM, like TSMC and Crossbar, have pivoted towards ReRAM because of its advantages compared to MRAM. EMASS has done the same, having informed investors in November 2024 that it is transitioning to ReRAM technology on its chips.

ReRAM uses resistance change in a material to store data, hence its name. The resistance is changed by forming/destroying a conductive path in a dielectric between two electrodes. The difference in resistance values between the states represents either a '0' or a '1'. ReRAM is very energy efficient and can scale down as transistors get smaller and smaller. Also helping the cause of ReRAM is how it uses materials that are more compatible with today's standard IC manufacturing as opposed to MRAM.

But even ReRAM has limitations with 10^6 write cycles before failure and this could potentially pose challenges for tasks such as 2D to 3D image conversion, AI image creation and deep learning. Nanoveu and EMASS (the company) have not yet specified the limit to which its ReRAM-powered EMASS technology can operate, but it has developed proprietary resilience mechanisms that significantly enhance ReRAM's durability and enable EMASS

EMASS is transitioning from MRAM to ReRAM, resulting in more efficient SoCs as a consequence.

to take advantage of ReRAM's unique comparative advantages without compromise. These include techniques such as fine-grained compute integration, endurance optimisation strategies, wear-levelling and error-correcting codes – designed to mitigate wear and extend ReRAM's operational lifespan.

Advanced data and AI model compression techniques are part of EMASS' secret sauce

Semiconductors are not all about memory units, controllers, accelerators and other hardware. Software is an integral part of computer chips. EMASS has developed some very lean software to support its advanced chip design:

- EMASS uses advanced compression techniques to reduce the memory requirements of the chip by getting rid of unnecessary weights, i.e. the weights used in the specific AI model on the chip.
- It then compresses the remaining weights in a smarter way in order to use fewer bits. Typically, other AI solutions use 8 or 16 bits, some can do it in 4 bits. EMASS has found a smarter way.

Compared to current industry practises, EMASS' approach is more dynamic when it comes to how many bits are used in its AI inference. At the start of an AI process, you typically process larger amounts of data and EMASS may use 6 or 7 bits in its processing. However, the number of bits used in processing can go down as the AI process for that particular data set progresses, so that towards the end of the computation cycle EMASS may only use 1 bit, or even less when, say, 3 weights are stored in 1 bit through compression.

Overall, EMASS' smart compression techniques substantially reduce the memory footprint in the SoC without impacting the accuracy of the AI inference.

Accuracy is maintained because there is no compression in the inference (computation). Before any calculation is done, the data is decompressed so the processor still sees the data as 8-bit data.

Once stored data is decompressed for processing, it is sent straight to the compute engine for processing rather than to an intermediate storage step (working memory/SRAM). The latter is typical for traditional computation processes.

By skipping this step, the EMASS SoC saves a lot of energy by not storing decompressed data in working memory.

EMASS has incorporated a specific hardware block in its chip design for this purpose (The AI weight decompressor in Figure 2). Each individual chip is in a package of 10mm x 10mm with a 0.8V supply voltage¹.

EMASS' energy preservation techniques are game-changing

The typical workflow in EMASS' AI inference process in Figure 2 takes compressed data from MRAM/ReRAM that is decompressed by the AI weight decompressor before it is sent straight to either Accelerator 1 (for 8 or 16 bit processing) or Accelerator 2 (just for 8-bit processing), depending on how big the layers (the number of weights in the AI model) are.

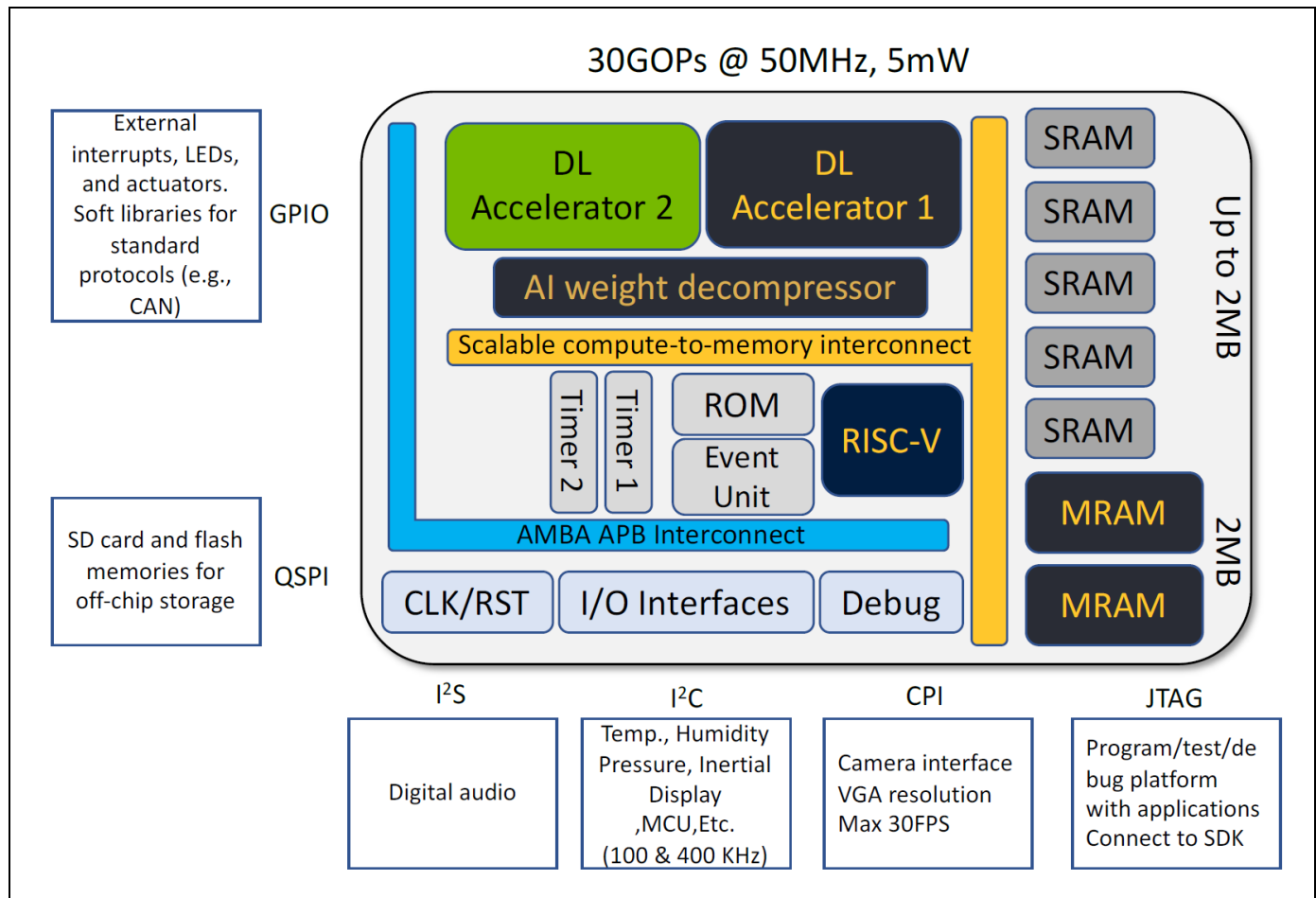
Advanced compression in the storage, not in the computation, guarantees accuracy.

¹ ECS-DoT Technical Brief (September 2023).



Any inference process done on EMASS' SoC will only use one accelerator at a time, which contributes to the very low energy consumption profile of the chip.

Figure 2: ECS-Dot functional block diagram



Source: Nanoveu

Once AI inference is completed, the resulting data is stored in the SRAM and can potentially be processed further in RISC-V if needed.

It is important to mention that when the chip is in data acquisition mode, i.e. an external event is being captured, all processing modules of the chip are shut off except for a very small part of the RISC-V core, which is a tremendous energy-saver as is illustrated in **Error! Reference source not found.**, that shows the key performance metrics of some of EMASS' main peers.

Energy preservation is a game-changer for battery-operated devices.

In more traditional chips, most modules will remain "awake" when not in use, which leads to much higher energy consumption. This is not such a big deal if the device is connected to a power point, but for any battery-operated electronic device needing AI inference, this specific feature of EMASS' SoC is a game-changer!



Figure 3: Performance metrics of EMASS' Edge AI peers

	EMASS	Perceive Ergo	GrAI Matter Labs	Flex Logix InferX	Analog Devices	Blaize Pathfinder
AI Capacity	30 GOPS @ 50 MHz, 2mW	500 GOPs @ 250 MHz, 75	1.5 TOPs, 2.5Watts	1-16 TOPs, 7-13 Watts	AI accelerators in DSPs	16-64 TOPs (varies)
Power Efficiency	Up to 12 TOPs/W	~6TOPs/W	0.6TOPs/Watt	~1-2 TOPs/W	Optimized for mixed-signal AI	~2-5 TOPs/W
Architecture	AI SoC + accelerator	Edge AI processor	Event based AI SoC	FPGA-based AI	Mixed-signal AI accelerators	GSP-based (Graph Streaming)
Memory	4MB MRAM	Unknown	Unknown	External DRAM	Integrated DSP/AI memory	4-16MB on-chip
Compressed AI Models	Sub-2-bit support	8-bit, 4-bit	NA	8-bit	Limited AI model	8-bit, some 4-bit
Process Node	22nm	22nm	28nm	16nm	Varies (older nodes)	12nm/16nm
Die Area	7mm ²	~49mm ²	64mm ²	~50mm ²	N/A	~40-60mm ²
Target Market	Ultra-low-power AI, Edge & IoT	Consumer AI (smartphones,	Robotics, low-power AI	Edge AI, FPGA acceleration	Industrial, audio, mixed AI	Automotive, industrial, cloud

Source: Pitt Street Research, Nanoveu

We have also looked at what we believe is EMASS' closest peer, Kinara, that was recently acquired by NXP Semiconductor (Figure 4).

Figure 4: Side by side comparison of Kinara's products with EMASS ECS-DoT

	Kinara Ara-1	Kinara Ara-2	EMASS ECS-DoT
Neural Cores	Flexible AI accelerator for vision applications	8 second-generation neural cores with custom ISA	General-purpose AIoT SoC with embedded AI cores
Dataflow Architecture	Dedicated dataflow engines for optimized tensor partitioning	Enhanced dataflow engines for improved routing and performance	Custom AI pipeline with on-chip power gating
Supported Data Types	INT8, FP16	INT4, MSFP16, INT8, FP16	INT8, FP16, and optimized low-bit data types
On-Chip Memory	Not officially disclosed (~128KB RAM listed in some sources)	4MB SRAM	1MB SRAM + 2MB MRAM (Non-volatile AI processing)
External Memory Support	1GB LPDDR4 DRAM	Up to 16GB LPDDR4/DDR4X per chip	Supports off-chip RRAM/MRAM/FLASH/nVSRAM via Parallel, SPI, or I2C interface
Max AI Model Size	1 Billion parameters (optimized for compact AI models)	Up to 30 Billion parameters in INT4	13 Million parameters (uncompressed format)
Chip Size	15mm × 15mm (FCBGA package)	17mm × 17mm (EHS-FCBGA package)	2.2mm × 3.4mm (Ultra-compact for Edge AI)
Fabrication Technology	28nm process	16nm process	≤22nm with integrated MRAM
Power Consumption	1.7W	6W	1.5mW (0.0015W)
Maximum Computation	5 TOPS	40 TOPS	30 GOPS (0.03 TOPS)
Efficiency (TOPS/W)	2.94 TOPS/W	6.67 TOPS/W	20 TOPS/W

Source: Pitt Street Research, Nanoveu

Horses for courses: Where EMASS shines compared to peers

Chip design is always a trade-off between energy consumption, performance, manufacturing cost, die size etc. In other words, there is not one chip to rule them all.

EMASS performs better in 5 key areas.

When we analyse the key performance metrics of EMASS' key peers, it is very clear that EMASS scores points in 5 key areas:

1. **Best power efficiency (12 TOPs/W):** Most competitors operate at 2-10 TOPs/W, meaning EMASS processes more AI workloads per watt, making it superior for battery-powered edge AI, wearables and IoT.
2. **Smallest die size (7mm² at 22nm resolution):** EMASS is much smaller than Blaize (~40-60mm²), Perceive (~25mm²) and GrAI Matter (~20mm²). This enables cost-effective, high-yield production and better scalability for mass deployment.
3. **Better compressed AI Model support (<2-bit models):** GrAI Matter, Perceive and Flex Logix rely on 4-bit and 8-bit models, but EMASS AI supports sub-2-bit AI models. This leads to higher computational efficiency and a lower memory footprint.
4. **No external DRAM required (4MB MRAM On-Chip, ReRAM soon):** Flex Logix and Blaize need external LPDDR4 DRAM, which increases cost, power consumption and latency. Additionally, EMASS' on-chip MRAM/ReRAM minimises latency and improves real-time processing.
5. **Balanced AI Performance (30 GOPS at 2mW):** EMASS has a lower absolute AI performance than Blaize (~64 TOPS), but is far more efficient, which is perfect for low-power edge AI, IoT and ultra-low-power devices.

EMASS peers perform better in these 3 areas solely due to the larger chip areas they provide which allows for more compute units or memory:

1. **Higher Raw AI Performance (Blaize and Flex Logix):** Blaize processes up to 64 TOPS with Flex Logix up to 16 TOPS. This is better for automotive and industrial AI inference at the Edge, i.e. high-end applications. However, EMASS' AI is focused on ultra-low-power applications, not high-end AI inference.
2. **Already adopted in market (Perceive and Analog Devices):** Perceive's Ergo is already inside consumer AI products (e.g. smartphones, smart home devices). Analog Devices has an established industrial and sensor AI ecosystem already. EMASS will need strong partnerships to compete in these markets.
3. **Better for high-memory AI tasks (Flex Logix and Blaize):** EMASS AI's 4MB MRAM/ReRAM is efficient, but limits large AI models. Flex Logix uses external DRAM and Blaize has up to 16MB on chip for larger AI workloads (like NLP, high-resolution vision AI etc).

Summarising the 8 performance metrics above, we can see that EMASS is by far the best solution for ultra-low-power AI at the Edge, i.e. for applications such as IoT, wearables, tinyML, always-on AI etc, which is exactly what it was designed for.

Flex Logix and Blaize are best suited to higher-performance AI in industrial, automotive or FPGA-based applications, while the Perceive and Analog Devices solutions perform best in consumer AI applications. EMASS was not designed for any of these applications.

In conclusion, EMASS' smart chip design, clever use of new NVM technology, enhanced memory compression techniques and highly efficient processing workflow have resulted in a high-potential, ultra-low-power SoC specifically for AI inference at the Edge of the Internet.

The market opportunity for EMASS is large and growing fast

Near term goal is to establish itself commercially in a few areas

EMASS' chip is fully functional, and has been tested and benchmarked. The chip architecture described above is scalable for bigger use cases, e.g. additional accelerators can be added to create a more powerful chip, for instance for autonomous driving, but for now EMASS is focussed on establishing itself from a commercial point of view with the current iteration of the chip.

Later on, when ReRAM becomes available in higher densities/larger modules, the company will likely also look at use cases that require substantially more powerful chips. At that time, it can add language models, video analytics etc as required by customers.

But there are many potential application areas for EMASS

EMASS could be useful for any device that processes data and that requires ultra-low energy consumption. This includes both existing devices, which can be embedded with AI capabilities without requiring excessive power or hardware upgrades, as well as the next generation of devices.

Examples include:

- **Security devices.** They could be enhanced with efficient, real-time object tracking and facial recognition, instant alerts and improved monitoring in busy or high-risk areas.
- **5G enabled IoT devices,** such as smart watches, medical implantable devices, smart glasses and lenses, biometric monitors, drones and smart agriculture. EMASS could enable the processing of live biometric data, such as oxygen, hydration, blood glucose levels or even facial analysis for identification purposes.
- **Medical imaging.** EMASS could improve the reach and portability of medical imaging devices. Diagnostic models could be improved by processing live biometric sensor feeds from multiple sources. There is potential to combine multiple radiological images to create coherent 3D images for smart-glasses and next-generation visual displays.
- **Realtime immersive AR/VR conversion from videos.** Delivering seamless and responsive interactions, making immersive environments more engaging and believable.
- **EyeFly3D (NVU's legacy business).** EMASS' ultra-low-power SoC's integrated with AI software developed by the company will allow for more efficient conversion of high resolution 2D images and videos to 3D, reducing latency and improving performance without excessive draining of the battery. This ensures high-quality 3D visuals, even on smaller, power-sensitive devices.

Many of these use cases are available today and so you may be forgiven for thinking technologies like EMASS' are a 'nice to have' rather than 'need to have'. But as devices and chips continue to shrink in size and increasing amounts of data need to be processed, more and more is demanded of computing devices. And the wait time back and forth to the Cloud will increasingly become an issue and will result in higher energy consumption. By

EMASS could be useful for any device that processes data and requires extreme energy efficiency.

making decisions 'at the Edge', better and quicker decisions will be made at lower power consumption levels.

Moreover, EMASS can be applied in newly emerging fields, such as remote robotic surgeries and autonomous vehicles.

EMASS' commercial model is standard in the chip industry

Initially, Nanoveu plans to embed EMASS' SoC's in EyeFly3D-enabled devices so that they work synergistically with the EyeFly3D software, delivering superior 3D experiences on small, power-sensitive devices.

However, we believe the market opportunity for EMASS in its own right, i.e. as a standalone semiconductor technology that can be licensed by third parties, is substantially more interesting for Nanoveu and its shareholders alike.

Similar to most semiconductor IP that is licensed by third parties, we see a licensing model for EMASS, where Nanoveu can commercialise its IP in three steps:

- 1) Non-recurring Engineering fees to assist licensees with the design and integration work,
- 2) One-off IP license fees, and
- 3) Recurring royalties based on third party sales volumes.

Given the direction the compute market is going, i.e. decentralised computing, moving towards the Edge and increasingly smaller devices, we believe EMASS has a very substantial market opportunity ahead.

The SOC market opportunity is massive

There are many estimates for how big the SoC market is right now and how big it could become over time. One estimate that Nanoveu has used is Market&Markets' prediction that it could be US\$206bn by 2029, up from US\$138bn in 2024. If realised, this would represent 8.3% CAGR growth over the next 5 years.

This is just one estimate, but most forecasters value the SoC market in excess of US\$100bn² and expect significant growth over the rest of the 2020s³.

Most estimates put the SOC market in excess of US\$100bn and expect CAGR growth of at least 8% up to 2030.

² See for instance estimates from Grand View Research, Transparency Market Research and System Market Research.

³ The 3 aforementioned firms all estimate CAGR growth of over 5% up to 2030.



Our valuation of Nanoveu is based on EMASS

In our valuation of Nanoveu, we have specifically looked at the EMASS side of the company given that we believe that is where substantially all of the shareholder value is likely to be created going forward.

Peer group valuation suggests significant upside for EMASS

The valuation of Nanoveu's ASX-listed peers can give us a good sense of the potential value of Nanoveu shares.

The average ASX-listed semiconductor company is capitalised at A\$195m (Figure 5). Granted, this does vary widely amongst companies because they are at different stages of development.

Indeed, exclude Weebit (ASX:WBT) and BrainChip (ASX:BRN) from the average and the average valuation drops to A\$82m. However, these two companies do illustrate what valuations ASX-listed semiconductor companies can achieve once they start to commercialise, which is why we include both stocks in our peer group.

**ASX semiconductor peers
valued >300% higher than
Nanoveu overall.**

Figure 5: Peer group valuation of ASX semiconductor stocks

Company	Ticker	#shares (m)	Share Price (A\$)	Market Cap (A\$ m)
4DS Memory	4DS	1,763.4	0.033	58.2
Archer Materials	AXE	254.8	0.325	82.8
AudioPixels	AKP	29.2	6.20	181.0
BluGlass	BLG	1,839.3	0.021	38.6
BrainChip	BRN	1,972.5	0.265	522.7
Adisyn	AI1	617.3	0.08	50.6
Weebit Nano	WBT	206.6	2.09	431.8
Average				195.1
Nanoveu (fully diluted)	NVU	1,146.7	0.042	48.2
Nanoveu valuation per share based on peer group valuation (fully dil.)				0.17

Source: Pitt Street Research

Valuation of A\$0.17 per share

Applying the average ASX semiconductor valuation in Figure 4 to Nanoveu, we arrive at a valuation of per share of A\$0.17 (fully diluted), implying >300% upside from the current share price, which is our initial valuation level for Nanoveu.

However, the average valuation for Weebit Nano and BrainChip is around A\$480m, or A\$0.42 per Nanoveu share, i.e. another level of valuation upside altogether.

This upside assumes Nanoveu can successfully finalise design, tape-out and qualification of EMASS' first product that would then be ready for commercialisation. In other words, this share price upside assumes the company can do what Weebit Nano and BrainChip have already done with their respective products, i.e. sign commercial deals for these products.

**Further upside if Nanoveu can
replicate the development
success of Weebit Nano and
BrainChip.**

***Strong appetite to acquire
Intellectual Property in the
Edge AI space.***

***Recent deal in EMASS' domain
valued takeover target Kinara
at nearly A\$500m.***

***Initial valuation of A\$0.17 per
share, but potentially with a lot
more upside in an M&A
scenario.***

Recent M&A activity signals strong demand for IP in Edge AI

As we noted in our [recent report on Adisyn \(ASX:AD1\)](#), we believe a Merger & Acquisition (M&A deal) is a realistic prospect for certain ASX-listed semiconductor stocks, including Nanoveu. Larger companies in the semiconductor and computer memory spaces are always on the lookout for new IP that can give them an advantage over their competitors.

The latest example in EMASS' domain is the acquisition on 10 February 2025 of Kinara by Dutch semiconductor manufacturer NXP Semiconductor (NASDAQ: NXPI, market cap US\$62bn). Edge AI company Kinara, based in Silicon Valley, provides high-performance AI for Edge devices and will be integrated in NXP's i.MX 8M and i.MX 9 processors for Automotive, Industrial, vision and Human/Machine Interfacing.

Kinara valued at nearly A\$500m

NXP is buying Kinara for US\$307m, which equates to A\$482m at current exchange rates. While EMASS has some way to go in terms of development as well as manufacturing, testing and qualification of demo chips, we believe the Kinara acquisition illustrates what the semiconductor industry is willing to pay for the right technology.

The A\$482m for Kinara is very close to Weebit Nano's and BrainChip's average valuation and it would equate to A\$0.42 per Nanoveu share. We believe these numbers underline the potential for Nanoveu if and when an M&A scenario materialises.

Conclusion: We value Nanoveu at A\$0.17 per share

Our initial valuation for Nanoveu is A\$0.17 per share, based on the average valuation of the ASX-listed semiconductor peer group, which includes companies with IP that is at various stages of development and commercialisation.

However, it is clear, in our view, that if Nanoveu can successfully get an initial commercial product across the finish line, i.e. ready for commercialisation, there is substantially more upside to the shares as illustrated by Weebit Nano and BrainChip.

And even prior to that time, as is illustrated by the Kinara acquisition, there is the potential for M&A activity that may see the EMASS IP acquired at a valuation that may be very substantially higher than today's share price.

Main share price catalysts

We see the following share price catalysts for Nanoveu shares:

- Development progress for EMASS SoC's, including final design, tape-out, manufacturing, testing and qualifying of demo chips.
- Sampling of FPGA's/demo boards by prospects, partners, collaborators etc.
- Partnership and collaboration announcements.
- Commercial deals for EMASS.



Risks

We see the following key risks to our investment thesis:

- **Funding risk:** Nanoveu will likely require external funding to support its commercialisation plans. Raising funds on favourable terms (both debt and equity) along with timeliness can be a key challenge for the company.
- **Regulatory risk.** The company's ability to commercialise its product is contingent on regulators maintaining approval where it already exists (including meeting ongoing regulatory compliance requirements) and giving approval to new products. A failure to give new products approval, or even a withdrawal of approval, could be catastrophic to its future ambitions.
- **Intellectual Property risk.** Key to the company succeeding will be the ability to protect its Intellectual Property. An inability to protect it will result in competitors being able to capitalise on the hard work Nanoveu has undertaken to get its products to market.
- **Key personnel risk:** There is the risk the company may lose key personnel and be unable to replace them and/or their contribution to the business.
- **Commercial risk.** There is the risk that the company may fail to execute its commercial objectives for a variety of reasons including:
 - i) The failure to find commercial partners,
 - ii) Supply chain issues,
 - iii) Lack of acceptance by the market,
 - iv) Competition.

Glossary

2D/Two Dimensional – The quality of being two-dimensional, just width and height

3D/Three Dimensional – The quality of being three dimensional, after the presence of the three spatial dimensions of width, height and depth.

Artificial Intelligence (AI) -

Accelerated Processing Unit (API) – A processor that combines a CPU and GPU (Central and Graphics Processing Units) onto a single chip.

Bandwidth – A measurement indicating the maximum capacity of a wired or wireless communications link to transmit data over a network connection in a given amount of time.

Cloud – A collection of remote servers, working together as a single ecosystem, enabling computing services.

Central Processing Unit (CPU) – The main component of a computer that executes instructions from software programs and controls other parts of the machine.

Cuprous – d

Edge computing – Computing where data is stored at the 'edge', on the data source, rather than in a centralised data centre or Cloud.

Giga operations – Technologies that enable computers to perform a variety of advanced functions.

GoPs – Clock speed x Instructions Per Cycle x Number of Cores

Milliwatts – A unit of power equal to a thousandth of a watt.

Magnetoresistive Random-Access Memory (MRam) – A non-volatile memory that stores data using magnetic domains.

Nano – In general terms, a unit prefix meaning on billionth. It is used as a short-hand term for nanotechnology or nanofabrication where the original root process alluded to is done at a smaller scale.

Nanoparticles – k

Nanofabrication – The art of fabricating structures or things at the nanometre range.

Nano Imprint Lithography (NIL) – A nanofabrication technique that creates nanometre-scale patterns with high resolution or low cost.

Resistive Random-Access Memory (ReRAM) – A type of Non-volatile computer memory.

Reduced Instruction Set Computing (RISC-V) – An open source Instruction Set Architecture (ISA) that is used to develop custom processors for a variety of applications.

System on a Chip (SoCs) - an integrated circuit that compresses all of a system's required components onto one piece of silicon.

Virtual Reality (VR) - a computer-generated environment with scenes and objects that appear to be real, making the user feel they are immersed in their surroundings.

Appendix I: The existing Digital Display business

Nanoveu's legacy business comprises of two technologies: EyeFly3D and Nanoshield.

EyeFly3D

EyeFly3D transforms 2D images onto regular digital displays into compelling 3D content without the need for special glasses.

EyeFly3D is a product comprised of a screen with nano-lenses (an active screen that is less than 0.1 millimetres thick) and software (the EyeFly3D) app. EyeFly3D transforms 2D images onto regular digital displays into compelling 3D content without the need for consumers to wear special glasses or content creators deploying expensive stereoscopic cameras. EyeFly3D software optimises 3D images for projection through specialised films to deliver distortion-free, brilliant 3D experiences – both 'organic 3D' rendered videos and photos, as well as those instantly converted from 2D.

The company initially developed its own software, but has developed proprietary AI algorithms for 2D to 3D conversion with Datature (3DAI).

How EyeFly3D works

EyeFly3D films are imprinted with thousands of mini lenses allowing overlay on digital displays without affecting touchscreen sensitivity, brightness or resolution.

EyeFly3D films are imprinted with hundreds of thousands of mini lenses allowing overlay on digital displays without affecting touchscreen sensitivity, brightness or resolution. The result is a compelling 3D experience on everyday digital displays with a broad range of commercialisation applications.

EyeFly3D is manufactured through a process known as Nano Imprint Lithography, a technique used to create nanoscale patterns in a low-cost and high-throughput fashion. Lithography generally involves drawing or printing a pattern on a smooth surface and then using a chemical reaction to 'fix' the image. NIL is lithography applied to nanoscale devices. It is particularly popular with semiconductor memory applications because it can produce resolutions better than 10 nanometres.

It is an optometric reality that a human's left eye sees different from the right eye. Nanolithography essentially tries to mimic that by miniaturised lenses embedded to the plastic. When light from LCD is transmitted, an algorithm to manipulate sub pixels is activated so that a stereoscopic image is created, sending the right image to right eye and the left image to left eye. However, the image appears as one - mimicking what we see in a 3D movie in theaters but with the glasses on the phone.

EyeFly3D's development history

EyeFly3D was initially developed in collaboration with a partner that spanned over a decade in China. The technology has been refined and perfected, delivering a better, brighter and more immersive 3D experience. This resulted in a new patent that protects the way the miniature lenses have been created - delivering distortion free lenses - even in ordinary mode. Several patents have recently been filed with Nanoveu's China partner, which whom Nanoveu has entered into a Joint Venture in Hong Kong – Fullveu Technologies (HK) Limited – to drive worldwide sales and marketing of the new and improved EyeFly3D product.

The recently improved EyeFly3D product will appear to be no different than an ordinary screen protector, but its uniqueness is at the nanoscale level, where the film consists of carefully shaped lenses patterned onto its surface. This patented innovation results in a smoother, clearer and more transparent finish compared to previously developed 3D filters.

Over time, the company increased its sales and enhanced the platform. In May 2024, NVU entered into an agreement with Singapore MLOps startup Datature to enhance the 3D image realism of NVU's 3D AI imaging platform for EyeFly3D, utilising monocular depth estimation technology that the company now owns. Also in May 2024, the company signed an exclusive distribution agreement for the South Korean market with Rahum Nanotech which would see 28,000 EyeFly3D screens to be supplied for Android and Apple iPhones from the initial order. US\$19.7m sales are targeted by December 2026. Finally, the company signed a collaboration and profit share arrangement with film and screen manufacturer Fullsand to sell EyeFly3D products and technologies globally, except in China, in a 51-49 Joint Venture. Using Fullsand's upgraded manufacturing capabilities, NVU hopes to adapt EyeFly3D to suit large format displays.

Use cases:

- **Video calls in 3D.** This may sound like a fantasy or a 'nice to have', but EyeFly3D could make it possible, and 3D video calls would be more interactive and intuitive than normal Facetime calls.
- **Big screen advertisements.** Companies can employ EyeFly3D technology on billboards to gain attention by having content jump out at you is important. This does need an extensive computer for every screen and is difficult to manage at this point in time, but as EyeFly3D continues to be developed, it could be adopted to larger 8K screens.
- **3D gaming.** 3D games exist, but most need users to wear 3D-glasses. EyeFly3D offers the prospect of being able to play these games without glasses.
- **3D content generally.** People will be able to capture 3D content with devices and share it with other phone users and the commercial path to market is through these large telcos. It is unlikely that EyeFly3D will be something people will watch full-length 3D films (not going to be a big traction even if it would be eventually possible). However, people will be more engaged with their own generated content, which can then be shared.
- **VR/AR.** This is a more longer-term use for EyeFly3D. But Virtual Reality/Virtual Reality is naturally 3 dimensional, and the VR/AR market is expected to undergo substantial growth over the rest of the decade – 27.5% CAGR⁴ according to Fortune Business Insights.

Revenue streams:

- **Screen Sales:** Sale of fully packaged products with installation kit, software and access to content.
- **Advertising:** In conjunction with the Software Development Kit, advertisers can turn their advertising campaigns into 3D with greater focus on their products
- **Digital Signage:** Technology can be expanded to include screens ranging up to 85 inches or larger.
- **Generative AI content:** NVU is current developing AI tools to automatically segment 2D content to 3D
- **Streaming:** When used in conjunction with AI tools and 3D cameras, glasses free 3D content can be viewed live, and users can be charged a monthly premium for this.

⁴ <https://www.grandviewresearch.com/industry-analysis/virtual-reality-vr-market>

EyeFly3D will have EMASS integrated going forward. But otherwise, the company intends to proceed with business in this division.

The commercial plan for EyeFly3D

As we have mentioned, EyeFly3D will have EMASS SoC's integrated going forward. But otherwise, the company intends to proceed with business in this division, with no current plans to divest.

Nanoveu has secured Rahum as an exclusive distribution partner in South Korea and is seeking partners in the rest of the world. Rahum is building a comprehensive entertainment ecosystem which will be integrating EyeFly3D. The Rahum deal is exclusive until 31 December 2026, subject to minimum order targets being met including:

- US\$1.05m in CY24
- US\$7.1m in CY25
- US\$11.25m in CY26

By 23 December 2024, Rahum provided orders to meet Minimum Order Quantity (MOQ) to retain exclusivity.

Nanoveu has also recently launched its latest smartphone apps for iOS incorporating a 2D to 3D monocular depth conversion enhancement. An Android version will follow soon. Users will have it delivered for under US\$35 and will be applied directly to Apple's iOS and Google's Android platforms.

Nanoshield Solar Coating

Nanoveu is revolutionising solar energy efficiency and operating cost reduction with several proprietary solar coatings (Figure 6). These cutting-edge coatings are designed to enhance solar panels and thermal absorbing mirrors performance, extend lifespan, and reduce maintenance costs.

Testing in the US in 2023 showed that Nanoshield Solar has an average power output boost of 25.4% over untreated solar panels⁵. Moreover, the company believes that Nanoshield Solar coatings are 10 times stronger than hydrogen-bridge bonds (commonly present in most other water repellent coatings)⁶.

Nanoshield Solar Coating:

- Transforms ordinary glass into a super hydrophobic, impact-resistant, and eco-friendly surface.
- Maintains maximum panel output for longer periods of time.
- Extends solar panel lifespan.
- Does not reduce transmissivity.
- Reduces maintenance costs, particularly the use of water.
- Withstands extreme weather conditions and environmental pollutants.

Applications:

- Photovoltaic solar panels.
- Concentrating solar thermal plants.

Key Benefits:

- Increased energy output.
- Reduced maintenance.
- Long-term durability.
- Sustainable and high-performance energy solutions.

⁵ ASX announcement 1 November 2023.

⁶ ASX announcement 7 June 2023.



Market Opportunity:

- As of Dec 2024, U.S. installed PV capacity stood at 187 GW or 374 million panels⁷. The installed capacity for the Middle East region was 22.3 GW or 46 million panels⁸ for the same period.
- Millions of solar panels and concentrating mirrors are in need of maintenance and upgrade as their efficiency declines with age and more severe weather conditions.
- High demand for solar maintenance solutions which can reduce water consumption and wear and tear on cleaning equipment.

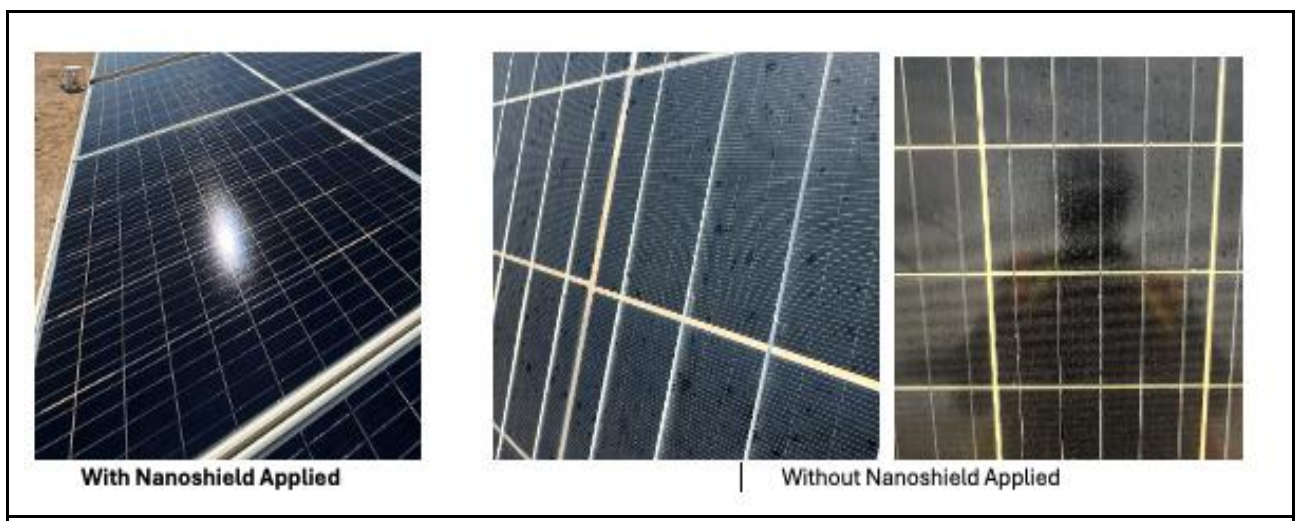
Competitive Advantage:

- Proprietary technology
- Proven results
- Strong customer base
- Extensive in-house R&D base

Growth Strategy:

- Focus on commercial and industrial solar markets
- Expand into new geographic markets
- Develop new coating applications
- Partner with leading solar energy companies

Figure 6: Nanoshield - Diamond Solar Coating, coated (left) and uncoated (right)



Source: Company

There is a significant opportunity in the US market.

There is a significant opportunity in the US market, with 187 GW of existing solar installations needing significant maintenance or upgrades. Nanoveu has identified a particular opportunity in the Middle East consisting of PV and concentrating mirrors and is currently in trials for its coatings. If adopted, this would provide significant revenue as there are millions of panels and mirrors in the region that require the Nanoshield solution that face energy loss because of fine sand accumulating on the panels resulting in a drop in electricity generation.

⁷ <https://seia.org/research-resources/us-solar-market-insight/>

⁸ <https://www.pv-magazine.com/2025/02/07/mena-region-on-track-for-75-gw-of-solar-by-2030>

Appendix II: Board and Management Team

Board of Directors & Management	
Name and Designation	Profile
David Pevcic Executive Chairman	<p>Dr David Pevcic is an experienced corporate professional and investor, with a principal focus on the resources and technology sectors. He is the Executive Director of ASX-listed Infini Resources Ltd (ASX:I88), Non-Executive Director of Battery Age Minerals Ltd (ASX:BM8) and founder of several privately owned mineral ventures.</p> <p>Dr Pevcic Holds a Bachelor of Science, Bachelor of Medicine and Bachelor of Surgery from the University of Western Australia.</p>
Alfred Chong Chief Executive Officer of Nanoveu	<p>Mr Chong is the founder of Nanoveu. He has three decades of experience in growing companies and executing trade sales in California and Singapore. Prior to Nanoveu, he was the Asia Pacific CEO for Atex Media Command, CEO for THISS Technologies Inc and 121View, and CMO at 3D International.</p> <p>The Singapore American Business Association named Mr Chong Entrepreneur of the Year and the San Francisco Chronicle named Alfred as one of the 20 foreign-born high technology visionaries who have helped to make the San Francisco Bay Area the world's technology centre. Mr Chong received both his Bachelor of Science in Computer Science and his MBA from the University of San Francisco.</p>
Dr Mohamed Sabry Aly Founder of EMASS	<p>Professor Aly is a Stanford-trained engineer whose has led pioneering research in SoC design. Professor Aly has led several major hardware initiatives, notably a ground-breaking \$25m project in Singapore and his work at Stanford University initiated a transformative \$75m DARPA program focused on emerging hardware technologies with new nanodevices. Additionally, his prolific contributions are reflected in over 50 published papers in top-tier conferences and journals, including Nature and the Proceeding of IEE.</p>
Mark Goranson CEO of Semiconductor Technology	<p>Mr Goranson has had a very extensive career in the global semiconductor industry, which includes 18 years at Intel as well as stints at ON Semiconductor, Freescale Semiconductor and TE Connectivity. Many of his roles have centered around chip manufacturing and commercialisation.</p>
Raymond Chen Chief Financial Officer	<p>Mr Chen has previously held senior management positions at Iluka Resources, NRW Holdings, Equinox Resources and KMPG. These roles encompassed Investor Relations, capital raising, treasury management and corporate transactions.</p>
Steven Apedaile Non-Executive Director	<p>Mr Apedaile has worked in the accounting profession for nearly 30 years, including 7 years with KPMG Hong Kong and 18 years with Horwath Hong Kong. Steven has experience in all facets of international business, corporate finance and forensic accounting services.</p> <p>Mr Apedaile is a founding director and a former managing director of an ASX listed company, a Fellow of the UK Institute of Chartered Accountants in England and Wales, and is a Member of the Australian Institute of Company Directors.</p>



Michael Winlo Non-Executive Director	<p>Dr Winlo has extensive experience in leading high-growth teams across the biotech, pharmaceutical and technology sectors, and is currently an Executive Director of Emyria Limited (ASX:EMD). Dr Winlo is also a Director and former CEO of Linear Clinical Research, a world-class provider of early and late stage pharmaceutical trials.</p> <p>Prior to this he was the health lead for Palantir Technologies (Silicon Valley), one of the world's largest big data companies. There, he led deployments for health and government organisations across the US and UK.</p> <p>Dr Winlo has a Master of Business Administration (MBA) from Stanford University and a Bachelor of Medicine, Bachelor of Surgery (MBBS) from the University of Western Australia.</p>
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Source: Company

Appendix III – Capital Structure

Security Class	Number	Percentage
Ordinary shares	742,430,227	65%
Options	235,295,256	21%
Performance rights	168,972,308	15%
Total	1,146,697,791	

Source: Company

Appendix IV – Patents and Technology Disclosures

Number	Title
1	Rate-distortion Optimised Coding for Deep Neural Network Compression
2	Edge SoC with AI acceleration
3	Porting of EMBED OS 5.12.4 to ECS-DOT's SoC and RISC-V CPU
4	Porting of the NVDLA ARM Linux Driver for EMBED-OS of ECS-DOT RISC-V CPU
5	Hardware design methodologies for efficient Tunstall Decoder
6	Register-Transfer-Level Implementation Of Decoders For Decoding A Codeword of a Tunstall Code
7	ShapoolNMS: Towards Scalable Hardware Acceleration of Non-Maximum Suppression for Object Detection

Source: Company

Appendix V – Analysts’ Qualifications

Marc Kennis has been an equities analyst since 1996.

- Marc obtained an MSc in Economics from Tilburg University, Netherlands, in 1996 and a postgraduate degree in investment analysis in 2001.
- Since 1996, he has worked for various brokers and banks in the Netherlands, including ING and Rabobank, where his focus has been on the technology sector, including the semiconductor sector.
- After moving to Sydney in 2014, he worked for several Sydney-based brokers before setting up TMT Analytics Pty Ltd, an issuer-sponsored equity research firm.
- In July 2016, with Stuart Roberts, Marc co-founded Pitt Street Research Pty Ltd, which provides issuer-sponsored research on ASX-listed companies across the entire market, including technology companies.

Nick Sundich is an equities research analyst at Pitt Street Research.

- Nick obtained a Bachelor of Commerce/Bachelor of Arts from the University of Sydney in 2018. He has also completed the CFA Investment Foundations program.
- He joined Pitt Street Research in January 2022. Previously he worked for over three years as a financial journalist at StockHead.
- While at university, he worked for a handful of corporate advisory firms.

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