PITT STREET RESEARCH

Adisyn Ltd.

Solving a major semiconductor bottleneck

Share Price: A$0.066

ASX:AI1

Sector: Technology

16 October 2025

Adisyn (ASX:AI1) is developing a graphene disposition technology that is intended to be applied to interconnects in computer chips, i.e. the nanoscale wires that connect individual transistors.

Interconnects made of graphene to the rescue

Today's transistor interconnects are largely made using copper, but they have reached the limits of where they can scale down to while remaining commercially viable. Other materials, with better electrical characteristics that are faster and produce less heat, are required to connect tomorrow's transistors if Moore's Law of ever-shrinking computer chips is to be followed. Enter 2D Generation, which was acquired by Adisyn in 2024.

Adisyn doesn't just have an alternative material (in graphene) that can scale down interconnects below 10 nanometers (nm), it is also working on a method to do this. Specifically, the company is using Atomic Layer Deposition (ALD) tools to work out the best way to deposit graphene on semiconductor wafers.

Major milestones are coming up

Adisyn expects to advance development of its graphene deposition "recipe" during the next 6 to 9 months and anticipates it will be able to deliver a demo prototype in 2026. It has been working with world-renowned semiconductor research institute imec and has been accepted into ConnectingChips, a development program that is part of the EU Chips Act that also involves NVDIA, the world's leading supplier of AI chips.

If Adisyn succeeds in delivering a full Proof Of Concept (POC), it will have solved a major fundamental bottleneck in the chip industry and a potential takeover by one of the major semiconductor equipment companies will be a distinct possibility, in our view. The recent commissioning of two ALD tools for R&D purposes is a major step towards achieving this goal, in our view.

We reiterate our valuation of A$0.29 per share

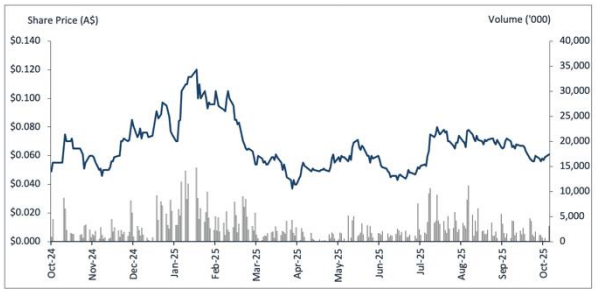
We reiterate our valuation for Adisyn of A$0.29 per share. This valuation uses a Sum-of-the-Parts for its two businesses: $0.22 for 2D Generation and $0.07 for the legacy business. We see potential for the company to re-rate from the current share price level as it continues the development of its graphene deposition technology. Meeting the next major milestone of having a demo prototype in 2026 will be crucial and the recent coming online of 2 ALD systems is an important step to meeting this. Please see page 10 for the key risks to our thesis.

Market cap. (A$ m)	47.9
# shares outstanding (m)[1]	725.6
# shares fully diluted (m)	1,125.1
Market cap ful. dil. (A$ m)	74.3
Free float	50.3%
52-week high/low (A$)	0.12 / 0.032
Avg. 12M daily volume ('1000)	2,821.9
Website	www.2dgeneration.com www.adisyn.com.au

Source: Company, Pitt Street Research

[1] Includes shares in escrow

Share price (A$) and avg. daily volume (k, r.h.s.)



Source: Refinitiv Eikon, Pitt Street Research

Sum-of-the-Parts Valuation	
Valuation 2D Generation (A$)	0.22
Valuation Services business (A$)	0.07
Overall Adisyn valuation (A$)	0.29

Source: Pitt Street Research

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Disclosure: Pitt Street Research directors own shares in Adisyn.

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Adisyn's critical process for next-gen computer chips

Adisyn is developing graphene-based computer interconnects, which connect individual transistors in chips.

Adisyn Ltd (ASX:AI1) consists of a namesake legacy business as well as semiconductor company 2D Generation that it acquired at the end of 2024. 2D Generation is developing graphene-based computer interconnects, which connect individual transistors in chips (Figure 1).

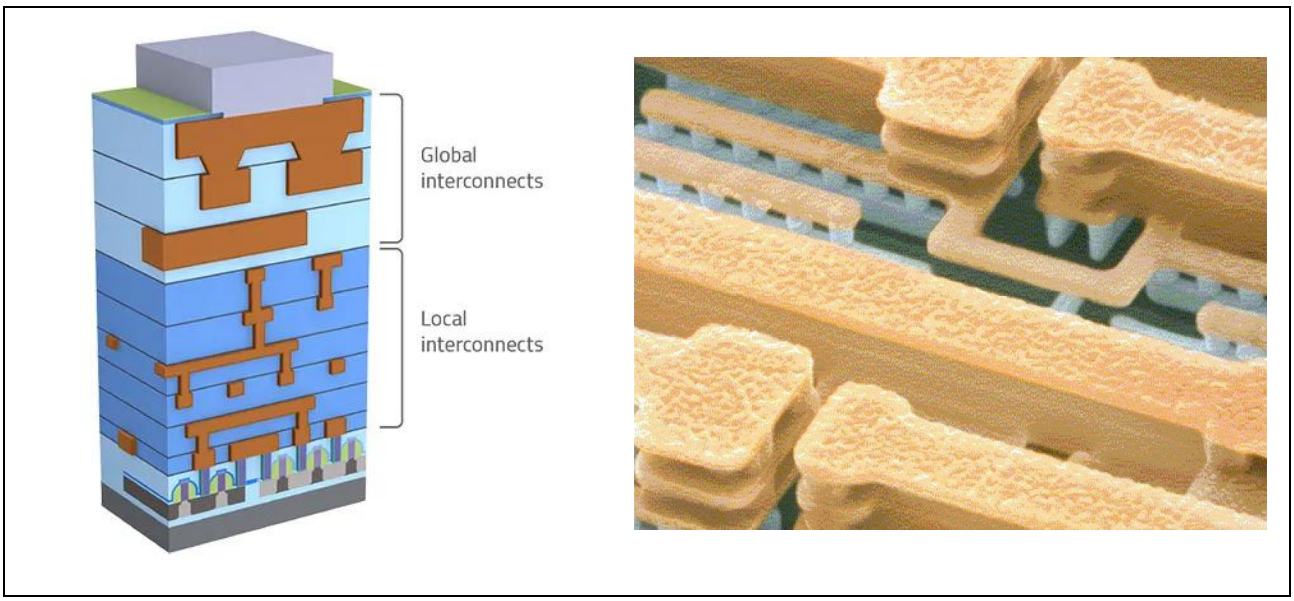
The problem that the company's graphene-based interconnects seek to overcome is that today's copper-based interconnects cannot continue to shrink in size while being expected to perform greater and greater feats – at least not without significant capital expenditure that rends it unviable. This is for a variety of reasons, including that copper's effective resistivity increases substantially as the electric wires that connect individual transistors shrink down below 10nm, which increases energy consumption and heat generation of the chips. Additionally, data transfer rates become more limited.

Transistor interconnects need to become a lot smaller

Today's most advanced transistors are mass-manufactured at 3nm and have copper interconnects that are between 10-15nm in width. But mass production of 2nm chips is ramping up as we speak, which will require local interconnects to go to 10nm and possibly a little smaller. We believe that will be where copper interconnects will run into their absolute limit.

Future production of sub-2nm transistors will most likely require a new type of material, such as graphene, to be used in interconnects.

Figure 1: Schematic of interconnects (LHS) and copper interconnects as seen through an electron microscope (RHS).



Source: Semiconductor Engineering and IBM

Adisyn is using ALD to build graphene interconnects

Graphene has not been the only solution proposed to solve the interconnect problem. Other possible materials that are being researched include nickel, cobalt, rhodium, iridium and ruthenium. It has also been proposed to change the way chips are manufactured to allow for wider circuitry to the transistors on the back of chips, although that would require significant changes to the manufacturing processes of major chip manufacturers that would be no more

cost-effective than investing capex into developing copper-based interconnects with ability to scale.

Graphene is looking very promising

Graphene has been proposed as a solution because of its high conductivity (even at very narrow linewidths), strength (200x stronger than steel) and its ability to be integrated into processes without significant changes to manufacturing processes.

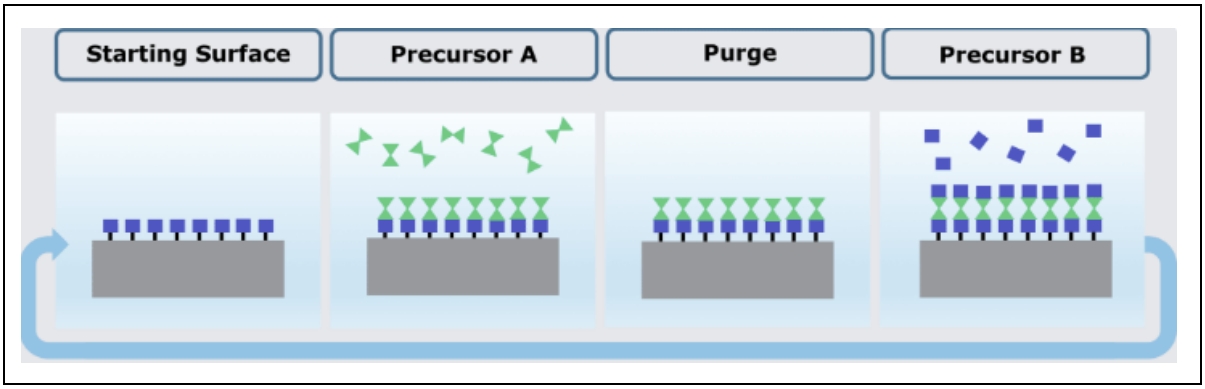
The challenge facing chip companies is manufacturing graphene and graphene layers in the first place. Adisyn does this through a method known as Atomic Layer Deposition (ALD). In ALD, chip manufacturers build a very thin (i.e. 1 atom thick) film, or layer, on a specific surface. Two reactant gasses enter the reaction chamber one at a time and this means that the reactions in the chamber stop by themselves once all so-called surface sites that a precursor can react with have been occupied (Figure 2). Any leftover precursor will literally just "hang around".

Once the reaction has stopped, the chamber is cleared (purged) of any leftover precursor gas and the second precursor is pumped in. Again, the reaction will stop by itself in the same manner. The result is a layer that is very thin, very uniform (which is good for chip performance).

Chip makers using ALD can build chips with a higher yield by making high-quality films and layers without risking damage to the underlying layers or substrates.

This process allows very precise control of thickness and can be done at more reasonable temperatures compared to other methods (350 degrees Celsius compared to the ~1,000 degrees needed for others). This low temperature in itself is a big win as it doesn't damage existing structures on the wafer that have been built in previous production steps.

Figure 2: The Atomic Layer Deposition process



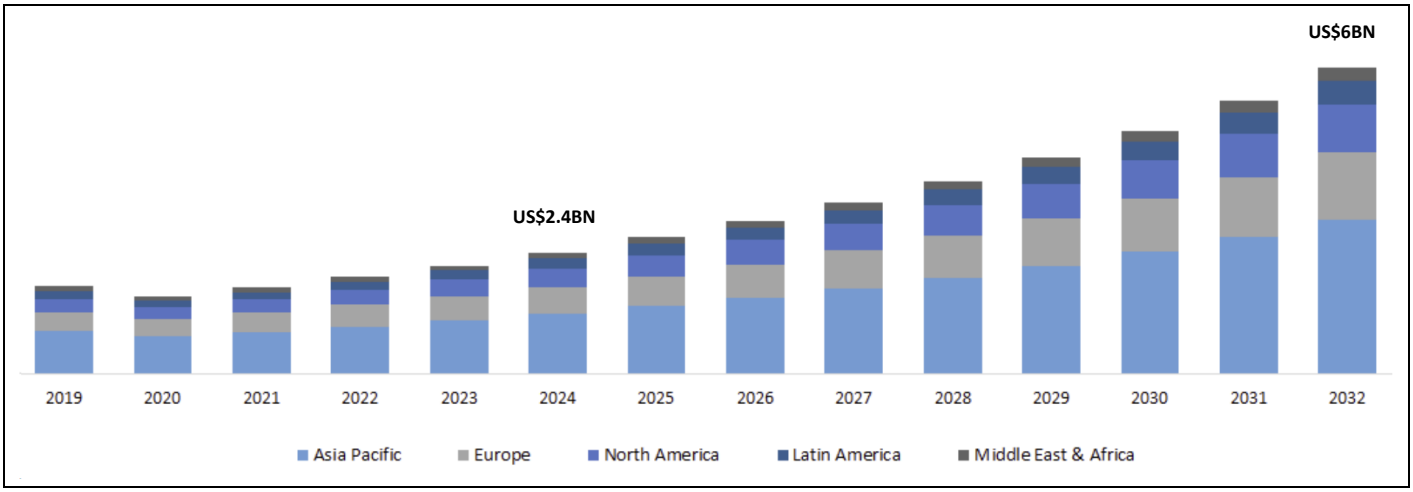
Source: Jynto/Wikimedia Commons

Why do chip makers need such a process? Using ALD tools, chip manufacturers can create high-quality films and layers without risking damage to the underlying layers or substrates, which improves overall yield, i.e. the number of total good (functioning) integrated circuits (ICs) on a wafer. And maximising yield is the ultimate goal in chip manufacturing, because that is the key driver of a fabrication facility's (fab) profitability.

Beyond the opportunity of high-end semiconductors, there are other opportunities 2D Generation's graphene deposition technology could potentially address in due course, including biomedical applications such as tissue engineering and drug delivery, in industrial coasting and in quantum computing (in lieu of silicon). But the ALD equipment market for

semiconductor manufacturing alone was worth US$2.4bn in 2024 and is expected to reach US$6bn by 2032 (Figure 3).

Figure 3: Atomic Layer Deposition market size (US$ BN)



Source: Polaris Market Research

2025: A big year for Adisyn so far

Adisyn is working with two ALD systems simultaneously.

In 2025, Adisyn has taken major steps in the development of its technology. In March, the company entered into a strategic partnership with the Jan Koum Centre for Nanoscience and Nanotechnology (TAU Nano Centre) at Tel Aviv University. Adisyn is leasing specialised equipment from the TAU Nano Centre, including the Beneq TFS 200 ALD system (Figure 4).

In parallel, the company has bought an ALD system of its own. 2DG received a customised model with specific capabilities for the company's graphene deposition process. These include a semi-automatic load lock enabling room-temperature sample exchange to reduce heating/cooling times and a reaction chamber suitable for wafer-scale processing.

Now that it has two machines, the company will be able to work in parallel across two systems and two industry standard environments. The development process will be able to proceed substantially faster than would otherwise be the case. This is not just because the company will be able to run multiple experiments at the same time, but also because it can simultaneously test diffusion barriers, precursors, reactants, surface treatments, temperatures, pressure controls and graphene-metal composites as well as graphene deposition on a range of metallic and non-metallic interconnect surfaces.

Figure 4: The Beneq TFS 200 ALD system that Adisyn is leasing.

Source: Company

The next steps

The ultimate aim of the current phase of the development is to identify at least 3 precursor candidates, and to determine optimal growth conditions and validating repeatability. In the first phase of activity, the company will develop and test the precursors by running them through the process that would be done in a commercial testing. The steps involved include (Figure 5):

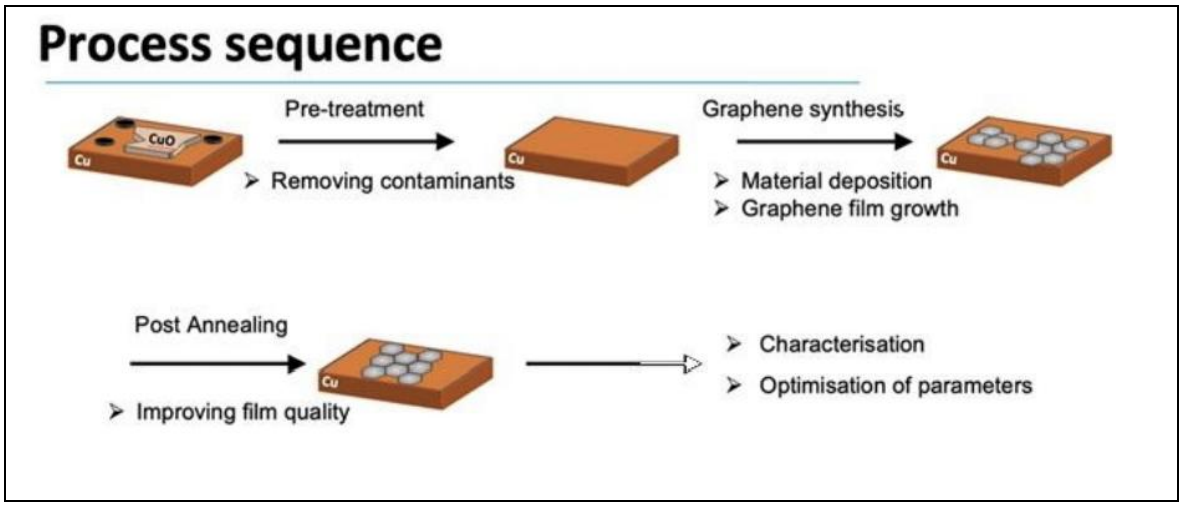
- Pre-cleaning the plasma so there is no contamination
- Mixing gases with selected organic precursors to co-react and form graphene films,
- Use annealing to enhance the crystalline quality and electrical properties of the graphene,
- Then evaluate the resulting films through rigorous testing, feeding into a continuous test-refine cycle to optimise growth parameters.

This R&D work will continue for the rest of 2025 and into Q1 2026. At that point, the company will move to a new phase of development focused on:

- Optimising pre-clean and deposition cycles for uniformity and yield,

- Assessing reproducibility of high-quality graphene growth,
- Moving to larger format substrates,
- Engaging partners for commercial trialling and joint development.

Figure 5: The process sequence



Source: Company

2026 should see a Demo Prototype

2D Generation aims to have a Demo Prototype ready by mid-2026.

2D Generation aims to have a Demo Prototype ready by mid-2026, i.e. proof that its technology is working on a 1x1cm chip.

The Demo Prototype should demonstrate that graphene interconnects can deliver the following characteristics:

- Graphene interconnects should **reduce signal delay** that is seen with copper interconnects.
- They should lead to **lower power consumption**, which in turn leads to,
- A **better heat profile**, i.e. less heat generation and better heat dissipation, which improves device performance and lifespan.
- Graphene interconnects need to facilitate **higher density of components** on an individual chip, such as transistors.
- Graphene interconnects should lead to **less crosstalk** between interconnections, i.e. less signal interference, which should result in higher, error-free data transfer rates.

2D Generation is already collaborating in the EU's ConnectingChips initiative.

Once a full Demo Prototype has been delivered, 2D Generation will seek collaborations in smaller projects to find application areas for its technology other than graphene interconnects. However, the company is currently already working with ConnectingChips, an initiative by the European Union (EU) aimed at driving innovation and collaboration in the semiconductor industry to make sure the EU stays at the forefront of the semiconductor industry. The company has already received grants for some of this work with more expected. In addition, 2D Generation may receive fees for non-recurring engineering work as part of this project.

Semiconductors already a US$600bn market and expected to be a US$1tn market by 2030

Demand for semiconductors has already surpassed US$600bn and will surpass $1tn by 2030.

According to a recent PWC report, demand for semiconductors has already surpassed US$600bn and will surpass US$1tn by 2030[1]. Key areas for demand will be from investments in servers and networks (to handle the increased demand that AI will place on them) as well as automotive, industrials, home appliances and computing devices. Even the eventual transition towards the next generation of mobile networks (6G) could see network speeds 200-100 times faster than 4G.

This growth means not just more chips, but better chips too

Obviously, this means there will be substantial investment in new semiconductor manufacturing fabs. Indeed, PWC estimates there will be US$1.5tn in investments between 2024 and 2030, which would be equal to investments seen in the previous two decades.

Investors have seen major players make major investments, such as TSMC, which is building a fab in Arizona that will see an investment of US$65bn initially, while additional phases will take the total to US$110bn.

Intel is investing US$20bn in its Ohio One mega-site and Samsung is investing US$17bn in a new plant in Texas. In Japan, TSMC is investing US$20bn into a facility near Kumamoto, which will be co-owned with minority partners, including NXP, Infineon and Bosch. In Europe, Infineon and STMicroelectronics are among the companies making major investments as well.

All this money is meant to meet the rising demand for semiconductors and to minimise geopolitical risk, i.e. reduce dependence on supply from China, but especially from Taiwan due to the threat China poses to Taiwan.

Graphene interconnects will help facilitate this growth

But more chips also means more transistors, both overall and in each individual chip, changes to chip architecture and new materials facilitating this. It is important for transistors to be high-speed, low-leakage and energy-efficient.

Graphene interconnects can solve the major interconnect issues copper is having at smaller resolutions.

As all this happens, interconnects will need to become much thinner (i.e. below 10nm as transistors go below 2nm) and the risk of heat density, electrical and thermal conductivity all become higher. These are pain points where the limitations of copper are becoming very apparent. But this also exactly the area where graphene-based interconnects come into play, thus representing a major opportunity for Adisyn in the next few years.

[1] PwC Semiconductor and beyond: Global semiconductor industry outlook 2026

Sum-of-the-Parts valuation of A$0.29 per share

We reiterate our valuation for Adisyn of A$0.29 per share.

We reiterate our valuation for Adisyn of A$0.29 per share under the current number of shares on issue. Of this, A$0.22 per share is attributable to 2D Generation and A$0.07 per share to Adisyn's legacy business. Please see our research initiation on Adisyn for more detail around our valuation.

We will briefly address the prospect of an M&A deal before 2D Generation's technology is fully developed. While we think an M&A deal in which 2D Generation is acquired by a semiconductor equipment OEM is a distinct possibility, we believe it is too early to speculate on a potential valuation in that scenario.

This is because semiconductor M&A transaction values are very volatile and cyclical, just like the broader industry is. The value will depend on the market sentiment at that time and how badly the acquirer wants to own 2D Generation's IP.

Nonetheless, we do think it is not unreasonable to speculate that it would most likely be a semiconductor equipment OEM, like Tokyo Electron, ASM International, Lam Research or Applied Materials rather than a semiconductor manufacturer given equipment makers would be able to derive the highest value from such an acquisition.

Potential share price catalysts

We see the following share price catalysts:

- We expect 2D Generation will have regular news flow around its graphene deposition development work in the near to medium term.
- Positive progress reports around the company's work with imec and the ConnectingChips collaboration.
- Possible announcements of additional semiconductor industry collaborations in the near to medium term.
- Delivery of Demo Prototype of graphene interconnects using ALD, expected in 2026.
- The legacy services business becoming profitable within the next 18 months.
- Potential takeover/divestment of either Adisyn's existing data centre business and/or 2D Generation in due course.

Risks

We see the following key risks to our investment thesis:

- **Funding risk**: Adisyn/2D Generation will require significant funding to realise its development and commercial ambitions. An inability to secure financing on favourable terms, or failure to secure funding at all, could be catastrophic for the company.
- **Technology risk**: There is the risk that the company may not move fast enough to keep pace with the competition. Additionally, in case 2D Generation's patents are infringed, there is no guarantee that the company can defends these patents in court given the substantial financial burden this would involve.
- **Cyber/Infrastructure risk**: A failure or interruption of the company's cyber systems or infrastructure systems could cause significant problems for the company's development program.

- **Commercial risk**. There is the risk that the company may fail to execute its commercial objectives for a variety of reasons including competition and lack of acceptance by the market.
- **Key personnel risk**: There is the risk the company may lose key personnel and may be unable to replace them and/or their contribution to the business

Appendix I – Patents

File Reference	Applicant	Application No.	Pub. No.	App Date	Title	Status
14801-US1	2D Generation Ltd Bar Ilan University (Ref. 7738-US)	18/574,061	US2024/0301554A1	29/6/2022	GRAPHENE COATED NON-METALLIC SURFACES, DEVICES AND METHOD THEREOF	Pending
14801-PC	2D Generation Ltd Bar Ilan University (Ref. 7738-WO)	PCT/IL2022/050701	WO2023/275873A1	29/6/2022	GRAPHENE COATED NON-METALLIC SURFACES, DEVICES AND METHOD THEREOF	National Phase
14802-US1	2D Genereation Ltd Bar Ilan University	18/692,223	N/A	20/9/2022	GRAPHENE COATED METALLIC SURFACES, DEVICES AND METHOD OF MANUFACTURE THEREOF	Pending
14802-PC	2D Genereation Ltd Bar Ilan University (Ref. 7744-WO)	PCT/IL2022/051010	WO2023/042210A1	20/9/2022	GRAPHENE COATED METALLIC SURFACES, DEVICES AND METHOD OF MANUFACTURE THEREOF	National Phase
14803-EP1	2D Genereation Ltd Bar Ilan University - 7754-PCT-EP	23708916.4	N/A	15/2/2023	METHOD OF MANUFACTURE OF GRAPHENE COATED SURFACES BY ATOMIC OR MOLECULAR LAYER DEPOSITION	Pending
14803-IL1	2D Genereation Ltd Bar Ilan University - 7754-PCT-EP	314976	314976	15/2/2023	METHOD OF MANUFACTURE OF GRAPHENE COATED SURFACES BY ATOMIC OR MOLECULAR LAYER DEPOSITION	Pending
14803-US1	2D Genereation Ltd Bar Ilan University - 7754-PCT-US	18/835,836	N/A	15/2/2023	METHOD OF MANUFACTURE OF GRAPHENE COATED SURFACES BY ATOMIC OR MOLECULAR LAYER DEPOSITION	Pending
14803-PC	2D Genereation Ltd Bar Ilan University - 7754-WO	PCT/IL2023/050158	WO2023156997A1	15/2/2023	METHOD OF MANUFACTURE OF GRAPHENE COATED SURFACES BY ATOMIC OR MOLECULAR LAYER DEPOSITION	Pending
14804-USP2	2D Genereation Ltd Bar Ilan University	63/690,518	N/A	4/9/2024	Graphene-Metal Complex	Pending

Source: 2D Generation

Appendix II – Analysts' Qualifications

Marc Kennis has been an equities analyst since 1996.

- Marc obtained an MSc in Economics from Tilburg University, Netherlands, in 1996 and a postgraduate degree in investment analysis in 2001.
- Since 1996, he has worked for various brokers and banks in the Netherlands, including ING and Rabobank, where his focus has been on the technology sector, including the semiconductor sector.
- After moving to Sydney in 2014, he worked for several Sydney-based brokers before setting up TMT Analytics Pty Ltd, an issuer-sponsored equity research firm.
- In July 2016, with Stuart Roberts, Marc co-founded Pitt Street Research Pty Ltd, which provides issuer-sponsored research on ASX-listed companies across the entire market, including technology companies.

Nick Sundich is an equities research analyst at Pitt Street Research.

- Nick obtained a Bachelor of Commerce/Bachelor of Arts from the University of Sydney in 2018. He has also completed the CFA Investment Foundations program.
- He joined Pitt Street Research in January 2022. Previously he worked for over three years as a financial journalist at StockHead.
- While at university, he worked for a handful of corporate advisory firms.

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